WEEKLY REPORT

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| Project: | New FPGA trace analyzer |
| Team member: | He Dai, Zhenning Jiang, Hui Li |
| Week ending: | Oct 24, 2014 |

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| He Dai |
| **Completed Deliverables:**   * AXI interface tutorial * GitHub tutorial * Chipscope Learning * ICON datasheet reading * Build basic circuits with bumper   **Time Spend:** total 20 hours  **Difficulties Encountered:**   * Chipscope learning(no license yet) * Time limited   **Activities to be started next week:**   * Trace Core Design with sample designs |

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| Zhenning Jiang |
| **Completed Deliverables:**   * Apply block ram IP generator and block ram control IP to write and read the data from Bram. (2 hours) * Build a basic system to test the function of bram and run simulation (12 hours) * Building Vivado in the Centos.(4 hours) * Read materials about JTAG and boundary scan technology.(3 hours)   **Time Spend:** 21 hours  **Difficulties Encountered:**   * The simulation takes long time to build the environment and there are some bugs in the ide tools.   **Activities to be started next week:**   * Block RAM IP Design and Driver IP Design |

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| Hui Li |
| **Completed Deliverables:**   * LabVIEW data socket and TCP/IP communication design (12 hours) * GitHub tutorial (3 hours) * Documentation(weekly report and PPT edit) (2 hour)   **Time Spend:** 17 hours  **Difficulties Encountered:**   * Set URL and address in communication.   **Activities to be started next week:**   * LabVIEW-GUI Prototype Design |